RISHABH JAIN

VLSI Engineer

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EXPERIENCE

SOFTWARE ENGINEER (Contractual Employee)

Xilinx Inc.

June 2018 – Present Hyderabad, India

- Designing C++/OpenCL based kernels for FPGA and Handling SDx Examples for SDAccel and SDSoC Environment.

ASSISTANT TRAINER FOR HEP

Mentor Graphics Pvt. Ltd.

May 2018 – June 2018 Noida, India

- Instructing Undergraduate students in the Professional Training for Verification of Electronic Designs using System Verilog.

DESIGN AND VERIFICATION ENGINEER TRAINEE

DKOP Labs Pvt. Ltd.

January 2018 – May 2018 Noida, India

- Industry—based training and hands—on experience of Front End VLSI domain using tcl/shell, Verilog and System Verilog.

HEP TRAINEE (DESIGN AND VERIFICATION ENGINEER)

Mentor Graphics Pvt. Ltd.

June 2018 – July 2018 Bangalore, India

- Selected amongst top 30 students across India.
- Verification of Electronic Designs (designed in Verilog) using Layered, Object Oriented Test benches in System Verilog.

EMBEDDED SYSTEM ENGINEER

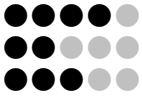
Gravity Innovations LLP

2018 March – December Delhi, India

- Working on machines and electronic circuits based on Embedded Micro-controllers using Robotics and Internet of Things.

TECHNICAL SKILLS

C/C++, Digital System Design
OpenCL, Makefile, Shell Scripting
Verilog/System Verilog, Python



SOFTWARE SKILLS

- QuestaSim Prime
- Xilinx SDx, Vivado, ISE
- Linux OS (Fedora/Ubuntu/CentOS)
- Tanner Tool, PSpice
- Proteus Pro ISIS

EDUCATION

Bachelor of Technology (Electronics & Communication)

Maharaja Agrasen Institute of Technology

2018 Delhi

- 76.48%

AISSCE (CLASS XII)

Bal Bharati Public School

2014 Brij Vihar, U.P.

- 89.6%

CLASS X

Bal Bharati Public School

2012 Brij Vihar, U.P.

- CGPA: 9.4/10

PROJECTS

PROTOCOLS DESIGNING & VERIFICATION

- UART IP, SPI, AMBA AHB & AXI—lite.

LZMA COMPRESSION MODULE FOR FPGA

- Designed Range Encoder Module of LZMA compression for VCU1525 Xilinx FPGA using HLS and SDx.

LC3 MICROCONTROLLER VERIFICATION

- Verifying LC3 Microcontroller using SV Testbench environment

2 STAGE PIPELINED ALU WITH FIFO DESIGNING & VERIFICATION

- Designing the 2 stage ALU along with FIFO and Analysing the coverage using SV & tcl scripts.

SMART DUSTBIN

- Automated interactive Dustbin with dynamic monitoring of the vacant space.

PUBLICATIONS

- R. Jain, H. Tulsani, A. Bansal, "A two- tier steganographic model based on (2,2)VCS and integer wavelet transform", in Preceding of The 5th International Conference on Computing for Sustainable Global Development organized by IEEE, pp. 4731-4734, (2018).